Technical data sheet

Xilinx XC4000EX Support

Leonardo version 4.03

- technology specific logic optimization
- Look-Up Table (LUT) mapping
- detection of clock enable logic (for CLB flip-flops and I/O flip-flops)
- mapping to input/output flip-flops (IOBs)
- global set-reset (GSR) logic support
  - ⇒ automatic detection
  - ⇒ user selection
- constraints driven timing optimization
- data path synthesis (through module generation)
  - ⇒ operators (adders, subtractors, multipliers, comparators, etc.)
  - ⇒ counter inferencing and implementation
  - ⇒ RAM inferencing and implementation
  - ⇒ LogiBLOX support
- automatic clock buffer insertion
- interface to Xilinx M1 software through XNF netlists
  - ⇒ FMAP/HMAP symbols in XNF
- passing timing constraints to Xilinx place and route through XNF (TimeSpecs)
- passing properties through XNF
- static timing analysis
- area and delay reporting (critical path reporting)

Leonardo and Galileo version 4.1 (2Q97)

- interface to M1 software through XNF and EDIF formats
  - ⇒ TimeSpecs
  - ⇒ FMAP/HMAP
  - ⇒ properties
- preservation of busses through EDIF, VHDL, Verilog
- packing logic into configurable logic blocks (CLBs)
- delay estimates for interconnects using wireloads, with results very close to post place and route numbers
- backannotation through Xilinx simulation primitives libraries (SIMPRIM libraries)
- timing library for XC4000XL family